ABSTRACT

A system for implementing Incremental Redundancy (IR) operations in a wireless receiver includes a baseband processor, an equalizer, a system processor, and an IR processing module. The baseband processor receives an analog signal corresponding to a data block and samples the analog signal to produce samples. The equalizer receives the samples from the baseband processor, equalizes the samples, and produces soft decision bits corresponding to the data block. The equalizer may be implemented as a distinct processing component or may be performed by the baseband processor or system processor. The system processor receives at least the soft decision bits and initiates IR operations. The IR processing module receives the soft decision bits of the data block and performs IR operations on the data block in an attempt to correctly decode a corresponding data block.